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L#	Hits	Search String	Databases
L1	28462	((digital or integrated) adj circuit$1) with (simulat$3 or verification or verify$3 or design)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	326	1 and ((configuration or definition) near2 file)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	221	1 and (bus near2 transaction$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	10	2 and 3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	537	2 or 3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L11	1	8 and ((test adj case$1) with parameter$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L12	87	1 and (generat$3 with (test adj case$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L13	12	12 and ((test adj case$1) with parameter$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L15	0	12 and (parameter$1 with (increas$3 or increment$2))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L17	10	1 and ((bus with parameter$1) with chang$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L18	11	1 and (bus with function with language$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L19	2	1 and (syntax with (reduce$1 or condense$1 or simplif$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	10	1 and (((configuration or definition) near2 file) with syntax)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	6	3 and (generat$3 with (test adj case$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	4	1 and ((bus near2 transaction$1) with rule$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L20	16	1 and (((configuration or definition) near2 file) with rule$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L21	3	1 and (generat$3 with (test adj case$1) with rule$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L22	0	6 and 13	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L6	53	3 and (bus with parameter$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L16	2	1 and ((bus with parameter$1) with (increas$3 or increment$2))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L23	0	12 and (parameter$1 with (stepwise))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L24	0	1 and (parameter$1 with (stepwise))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L25	1412	1 and (parameter$1 with (step$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L26	635	1 and (parameter$1 with (increas$3 or increment$2))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L27	251	25 and 26	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L28	0	12 and 27	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L29	21	3 and 27	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L31	0	30 and ((bus near2 transaction$1) or (test adj case$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L30	63	1 and (parameter$1 with (increas$3 or increment$2) with step$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L32	4	1 and ("bus functional language")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L33	5	bus functional language	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L8	23	7 and (generat$3 with (test adj case$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L34	53	3 and (bus with parameter$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L1	28503	((digital or integrated) adj circuit$1) with (simulat$3 or verification or verify$3 or design)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	0	1 and "bus function language"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	4	5,867,400.pn. or 6,173,243.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	0	3 and "bus function language"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	3	3 and "language"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L6	11	bus near2 function$2 near2 language	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

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Results of search set L10:((((digital or integrated) adj circuit$1) with (simulat$3 or verification or verify$3 or design)) and (bus near2 transaction$1)) and (bus with parameter$1)

Document	Kind Codes	Title	Issue Date	Current OR	Abstract
US 20030201918	A1	Method and apparatus for adaptive bus coding for low power deep sub-micron designs	20031030	341/50	
US 20030115564	A1	Block based design methodology	20030619	716/8	
US 20030101307	A1	System of distributed microprocessor interfaces toward macro-cell based designs implement	20030529	710/305	
US 20030085768	A1	Phase locked loop reconfiguration	20030508	331/100	
US 20030070030	A1	Automatic corner case search in multi-agent bus interface verification	20030410	710/309	
US 20020186597	A1	Method and apparatus for adaptive address bus coding for low power deep sub-micron desig	20021212	365/200	
US 20020184419	A1	Asic system architecture including data aggregation technique	20021205	710/100	
US 20020166098	A1	Block based design methodology	20021107	716/1	
US 20020103950	A1	Bus transaction verification method	20020801	710/65	
US 20020073380	A1	Block based design methodology with programmable components	20020613	716/1	
US 20020065641	A1	Method and apparatus for encoding and generating transaction-based stimulus for simulation	20020530	703/17	
US 20020016952	A1	Block based design methodology	20020207	716/18	
US 20010042237	A1	Block based design methodology	20011115	716/8	
US 20010039641	A1	Block based design methodology	20011108	716/8	
US 20010018756	A1	Block based design methodology	20010830	716/1	
US 20010016933	A1	Block based design methodology	20010823	716/1	
US 6741190	B2	Method and apparatus for adaptive bus coding for low power deep sub-micron designs	20040525	341/50	
US 6725432	B2	Blocked based design methodology	20040420	716/4	
US 6718411	B2	Asic system architecture including data aggregation technique	20040406	710/100	
US 6701504	B2	Block based design methodology	20040302	716/10	
US 6698002	B2	Blocked based design methodology	20040224	716/4	
US 6694501	B2	Block based design methodology	20040217	716/10	
US 6684277	B2	Bus transaction verification method	20040127	710/100	
US 6636907	B1	Transferring data between asynchronous devices	20031021	710/25	
US 6631470	B2	Block based design methodology	20031007	716/3	
US 6629293	B2	Block based design methodology	20030930	716/4	
US 6622207	B1	Interpolation looping of prioritized audio samples in cache connected to system bus	20030916	711/118	
US 6621353	B2	Phase locked loop reconfiguration	20030916	331/1A	
US 6594800	B2	Block based design methodology	20030715	716/1	
US 6583735	B2	Method and apparatus for adaptive bus coding for low power deep sub-micron designs	20030624	341/51	
US 6581194	B1	Method for reducing simulation overhead for external models	20030617	716/4	
US 6574778	B2	Block based design methodology	20030603	716/1	
US 6567957	B1	Block based design methodology	20030520	716/4	
US 6460174	B1	Methods and models for use in designing an integrated circuit	20021001	716/18	
US 6393500	B1	Burst-configurable data bus	20020521	710/35	
US 6321285	B1	Bus arrangements for interconnection of discrete and/or integrated modules in a digital syster	20011120	710/306	
US 6269467	B1	Block based design methodology	20010731	716/1	
US 6173243	B1	Memory incoherent verification methodology	20010109	703/14	
US 6154801	A	Verification strategy using external behavior modeling	20001128	710/119	
US 6138207	A	Interpolation looping of audio samples in cache connected to system bus with prioritization ar	20001024	711/118	
US 6088753	A	Bus arrangements for interconnection of discrete and/or integrated modules in a digital syster	20000711	710/306	
US 6081864	A	Dynamic configuration of a device under test	20000627	710/100	
US 6073194	A	Transaction based windowing methodology for pre-silicon verification	20000606	710/100	

US 6016525 A	Inter-bus bridge circuit with integrated loopback capability and method for use of same	20000118	710/100
US 5983306 A	PCI bridge with upstream memory prefetch and buffered memory write disable address range	19991109	710/310
US 5983303 A	Bus arrangements for interconnection of discrete and/or integrated modules in a digital syster	19991109	710/315
US 5948089 A	Fully-pipelined fixed-latency communications system with a real time dynamic bandwidth allo	19990907	710/107
US 5752002 A	Method and apparatus for performance optimization of integrated circuit designs	19980512	703/14
US 5680643 A	Data bus including address request line for allowing request for a subsequent address word c	19971021	710/35
US 4825438 A	Bus error detection employing parity verification	19890425	714/56
US 4734909 A	Versatile interconnection bus	19880329	370/462
US 4326813 A	Dot matrix character printer control circuitry for variable pitch printing	19820427	358/1.8
US 20020103950 A	Automatic bus transaction verification method for ASIC, involves executing checking program	20040127	